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Srishyla Educational Trust (R)

GM INSTITUTE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Activity Report
on
"3- days Faculty Development Program (FDP) on Cadence Virtuoso Platform"

from

06/10/22 to 08/10/22

Resource Person/s

Mr. ShivaPrasad B K
Field Application Engineer
Entuple Technology, Bangalore – 588002

Deepika.V.B

Event coordinators
Mr. Santhosh B G/ Ms. Deepika V B
Assistant Professor

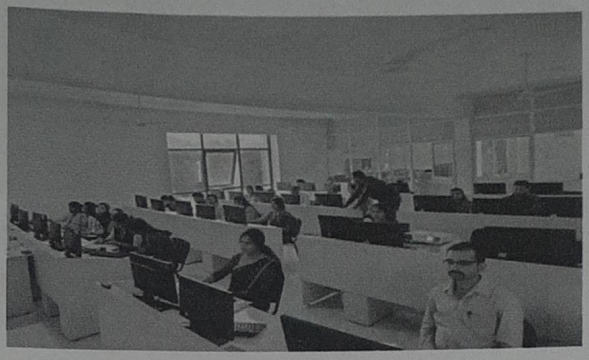
Verified By
Dr. Praveen J
Head of the Department

Checked by
Dr. Sunil Kumar B S
Dean Academics

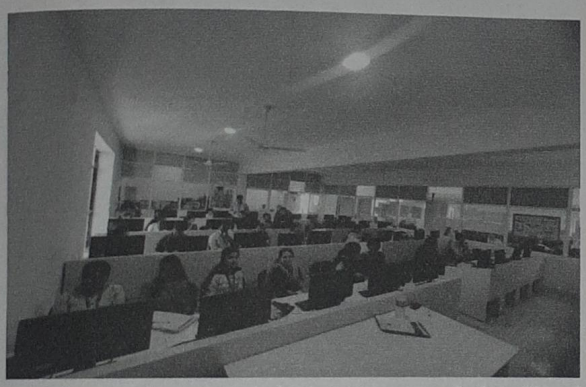
Checked by
Dr. Praveen J
IQAC-Director

Approved by
Dr. Y. Vijay Kumar
Principal

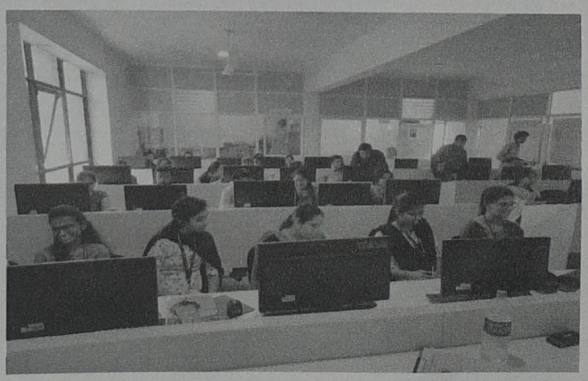
Report On "3-Days Faculty Development Program (FDP) on Cadence Virtuoso Platform"



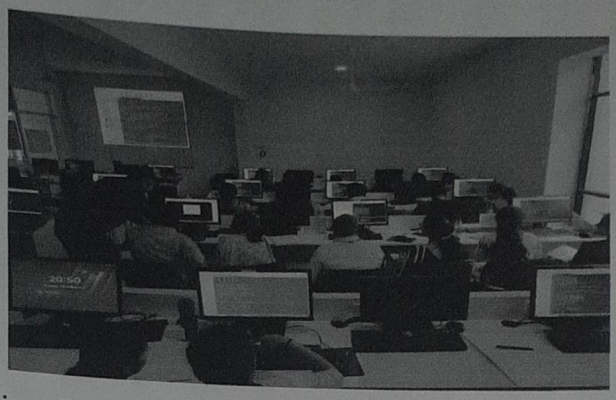
The Department of Electronics and Communication Engineering, GM Institute of Technology, Davangere organized a **"3-Days Faculty Development Program (FDP) on Cadence Virtuoso Platform"** by the resource person **Mr. Shivaprasad B K,** Sr. FAE, Entuple Technologies Pvt Ltd, Bangalore from 6th October 2022 to 8th October 2022 at 9.30 am to 5.00 pm in VLSI Lab.



Dr. Y. Vijaya kumar, Principal was presided over the Workshop. and address the students about the importance of the workshop to faculties and students. **Dr. Praveen J,** Profeesor & Head, Convener, ECE department welcomed the gathering and also briefed the assembled members about the importance of the Workshop topic in VLSI research field. The faculty members of ECE and the students of ECE were present in the Workshop.



The key note speaker of the Workshop Mr. Shivaprasad B K, started the presentation by giving introduction about the VLSI, usage and scope of Cadence tool in



Academics as well as in Industry. Cadence Virtuoso Platform. He also gave technical importance of Cadence tool , he also conducted Hands on Session for designing and simulating combinational & sequential digital circuit using Verilog HDL, Synthesis process of Digital circuits, Performed ASIC Design flow, Evaluation of synthesis reports to obtain optimum gate level Net List, design and simulate basic CMOS circuit and performed RTL-GDSII flow.

The resource persons encouraged all the faculty members and students by giving awareness about importance of Cadence Virtuoso Platform in VLSI research field in both Academics and Industry to build their Career. The faculties and students were motivated and benefited.

Srishyla Educational Trust (R), BheemaSamudra

GM INSTITUTE OF TECHNOLOGY, DAVANGERE

Department of Electronics and Communication Engineering

Certificate of Participation

This is to certify that Mr/Ms._____ has Participated in the IQAC initiative *"3-Days Faculty Development Program (FDP) on Cadence Virtuoso Platform"* organized by the Department of Electronics and Communication Engineering in association with EnTuple Technologies, Bengaluru from 6th to 8th October 2022.

MR. SHIVAPRASAD B K ENTUPLE TECHNOLOGIES	DR. PRAVEEN J CONVENOR & HOD	DR.Y.VIJAYAKUMAR PRINCIPAL